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EXAMINER	
VAN, LUAN V	

ART UNIT	PAPER NUMBER
1753	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,106	BONKABETA ET AL.	
	Examiner	Art Unit	
	Luan V. Van	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) *47* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) 1-47 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Receipt is acknowledged of papers submitted, which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9, 14-16, 18-22, 24-30, 35-41, and 43-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Taylor et al. '384.

Regarding claims 1, 3-5, 7, 9 and 14, Taylor et al. '384 teach a method of forming a layer of metal on a semiconductor structure, comprising: bringing an electrode into contact with an electrolyte (column 9 lines 63-66); bringing said semiconductor structure into contact with said electrolyte (column 9 lines 63-66); applying in a first time interval a

first current flowing from said electrode through said electrolyte to said semiconductor structure, said first current having a first amperage comprising a plurality of first positive pulses and a plurality of first negative pulses, an integral of said first amperage over said first time interval having a first value greater than zero (column 9 lines 22-35); and applying in a second time interval a second current flowing from said electrode through said electrolyte to said semiconductor structure, said second current having a second amperage, an integral of said second amperage over said second time interval having a second value less than zero (column 9 lines 22-35). Specifically, Taylor et al. '384 teach "a number of cathodic and anodic pulses with defined pulse widths may make up one group of pulses, which is then repeated. Typically such a group would include one or more cathodic pulses and at least one anodic pulse" (column 9 lines 22-35). An integral of the amperage (or cathodic charge transfer density as referred to by Taylor et al. '384) would inherently have a value greater than zero when net deposition of metal on the surface occurs (cathodic process). Likewise, an integral of the amperage would inherently have a value less than zero when dissolution of metal on the surface occurs (anodic process).

Regarding claim 2, Taylor et al. '384 teach "the cathodic-to-anodic net charge ratio will be greater than one, in order to provide a net deposition of metal on the surface" (column 9 lines 22-35). An absolute of said first value is greater than an absolute of said second value, since there is a net deposition of metal on the surface.

Regarding claims 6 and 8, Taylor et al. '384 teach pulses have a substantially rectangular shape (figure 1).

Regarding claims 15-16, Taylor et al. '384 teach a thin conducting layer (ie, seed layer) is applied (e.g., by PVD) over the entire surface of the element to provide electrical conductivity for the electroplating step (column 9 lines 55-62).

Regarding claim 18, Taylor et al. '384 teach chemical mechanical polishing said semiconductor structure (column 10 lines 51-57).

Regarding claims 19 and 39, Taylor et al. '384 teach a method, comprising: providing a semiconductor structure comprising at least one recess and at least one elevation (figure 3); electroplating said semiconductor structure for depositing a layer of metal on said semiconductor structure and for filling said at least one recess (column 11 lines 65-67) with said metal; electropolishing said semiconductor structure for preferentially removing said metal from said at least one elevation (column 10 lines 20-38); and chemical mechanical polishing said semiconductor structure, said chemical mechanical polishing removing a surplus of said metal from said at least one elevation and planarizing a surface of said semiconductor structure (column 10 lines 51-57).

Regarding claims 20-22, 24-25, 27-29, and 35-38 Taylor et al. '384 teach a method of forming a layer of metal on a semiconductor structure, comprising: bringing

an electrode into contact with an electrolyte (column 9 lines 63-66); bringing said semiconductor structure into contact with said electrolyte (column 9 lines 63-66); wherein said electroplating is performed by applying in a first time interval a first current flowing from said electrode through said electrolyte to said semiconductor structure, said first current having a first amperage comprising a plurality of first positive pulses and a plurality of first negative pulses, an integral of said first amperage over said first time interval having a first value greater than zero (column 9 lines 22-35); and wherein said electropolishing is performed by applying in a second time interval a second current flowing from said electrode through said electrolyte to said semiconductor structure, said second current having a second amperage, an integral of said second amperage over said second time interval having a second value less than zero (column 9 lines 22-35). Specifically, Taylor et al. '384 teach "a number of cathodic and anodic pulses with defined pulse widths may make up one group of pulses, which is then repeated. Typically such a group would include one or more cathodic pulses and at least one anodic pulse" (column 9 lines 22-35). An integral (or cathodic charge transfer density as is referred to by Taylor et al. '384) would inherently have a value greater than zero when net deposition of metal on the surface occurs, since the process is cathodic. Likewise, an integral would inherently have a value less than zero when dissolution of metal on the surface occurs, since the process is anodic. Furthermore, Taylor et al. '384 teach "one skilled in the art will recognize that the point in time chosen as the initial point of the pulse train is entirely arbitrary. Either the cathodic pulse or the anodic pulse (or any point in the pulse train) could be considered as the initial point" (column 8 lines

14-19). Therefore, any cathodic pulses can be considered as either the first pulse(s) or the second pulse(s), and any anodic pulses can be considered as either the first pulse(s) or the second pulse(s).

Regarding claims 26 and 30, Taylor et al. '384 teach the pulses have a substantially rectangular shape (figure 1).

Regarding claims 40-41, Taylor et al. '384 teach a thin conducting layer (ie, seed layer) is applied (e.g., by PVD) over the entire surface of the element to provide electrical conductivity for the electroplating step (column 9 lines 55-62).

Regarding claims 43-46, Taylor et al. '384 teach "a number of cathodic and anodic pulses with defined pulse widths may make up one group of pulses, which is then repeated. Typically such a group would include one or more cathodic pulses and at least one anodic pulse" (column 9 lines 22-35). Furthermore, Taylor et al. '384 teach "one skilled in the art will recognize that the point in time chosen as the initial point of the pulse train is entirely arbitrary. Either the cathodic pulse or the anodic pulse (or any point in the pulse train) could be considered as the initial point" (column 8 lines 14-19). Therefore, whenever one group of pulses comprising of cathodic pulses is repeated (for example, a second group of pulses), electroplating would occur on a semiconductor structure for increasing a thickness of a metal layer; and electroplating is performed after electropolishing whenever the cathodic pulses are preceded by the anodic pulses

(as with a second group of pulses). Further, electropolishing is performed after electroplating whenever the cathodic pulses are followed by the anodic pulses.

Claims 1-9, 14-15, 18-30, 35-40, and 43-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Taylor '144.

Regarding claims 1, 3-5, 7, 9 and 14, Taylor '144 teaches a method of forming a layer of metal on a semiconductor structure, comprising: bringing an electrode into contact with an electrolyte (claim 1); bringing said semiconductor structure into contact with said electrolyte (claim 1); applying in a first time interval a first current flowing from said electrode through said electrolyte to said semiconductor structure, said first current having a first amperage comprising a plurality of first positive pulses and a plurality of first negative pulses, an integral of said first amperage over said first time interval having a first value greater than zero (figure 1); and applying in a second time interval a second current flowing from said electrode through said electrolyte to said semiconductor structure, said second current having a second amperage, an integral of said second amperage over said second time interval having a second value less than zero (figure 1).

Regarding claim 2, Taylor '144 teaches "the cathodic-to-anodic net charge ratio will be greater than one, in order to provide a net deposition of metal on the surface"

(column 5 lines 15-23). An absolute of said first value is greater than an absolute of said second value, since there is a net deposition of metal on the surface.

Regarding claims 6 and 8, Taylor '144 teaches pulses have a substantially rectangular shape (figure 1).

Regarding claim 15, Taylor '144 teaches a thin conducting layer (ie, seed layer) is deposited over the entire surface of the element to provide electrical conductivity for the electroplating step (column 3 lines 45-57).

Regarding claim 18, Taylor '144 teaches chemical mechanical polishing said semiconductor structure (example 1).

Regarding claims 19 and 39, Taylor '144 teaches a method, comprising: providing a semiconductor structure comprising at least one recess and at least one elevation (column 3 lines 35-45); electroplating said semiconductor structure for depositing a layer of metal on said semiconductor structure and for filling said at least one recess (column 3 lines 35-45) with said metal; electropolishing said semiconductor structure for preferentially removing said metal from said at least one elevation (figure 1, profile 4); and chemical mechanical polishing said semiconductor structure, said chemical mechanical polishing removing a surplus of said metal from said at least one elevation and planarizing a surface of said semiconductor structure (example 1).

Regarding claims 20-25, 27-29, and 35-38 Taylor '144 teaches a method of forming a layer of metal on a semiconductor structure, comprising: bringing an electrode into contact with an electrolyte (claim 1); bringing said semiconductor structure into contact with said electrolyte (claim 1); wherein said electroplating is performed by applying in a first time interval a first current flowing from said electrode through said electrolyte to said semiconductor structure, said first current having a first amperage comprising a plurality of first positive pulses and a plurality of first negative pulses, an integral of said first amperage over said first time interval having a first value greater than zero (figure 1, profiles 1-3); and wherein said electropolishing is performed by applying in a second time interval a second current flowing from said electrode through said electrolyte to said semiconductor structure, said second current having a second amperage, an integral of said second amperage over said second time interval having a second value less than zero (figure 1, profiles 1-4).

Regarding claims 26 and 30, Taylor '144 teaches the pulses have a substantially rectangular shape (figure 1).

Regarding claim 40, Taylor '144 teaches a thin conducting layer (ie, seed layer) is deposited over the entire surface of the element to provide electrical conductivity for the electroplating step (column 3 lines 45-57).

Regarding claims 43-46, Taylor '144 teaches electroplating on a semiconductor structure for increasing a thickness of a metal layer (figure 1, profiles 2-3); and electroplating is performed after electropolishing (figure 1, profile 1-3). Further, electropolishing is performed after electroplating (figure 1, profile 1-4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 10-13 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. '384 in view of Piersol.

Taylor et al. '384 teach the method as described above in addressing claims 1 and 19-20. Although Taylor et al. '384 does not explicitly teach using sinusoidal waveform, the reference suggest that this can be used, stating "the waveform need not be rectangular as illustrated. The cathodic and anodic pulses may have any voltage-time (or current-time) profile. In the following discussion rectangular pulses are assumed for simplicity" (column 8 lines 9-14).

Nevertheless, using sinusoidal waveform for electroplating is well known in the art. For example, Piersol teach that by using sinusoidal waveform, "the rate of evolution of hydrogen is varied frequently and suddenly, and the gradual accumulation of hydrogen at the cathode surface is obviated. The troublesome sudden variations in plating conditions caused by such accumulations are likewise obviated" (pg. 2 lines 88-95).

Furthermore, modifying the parameters of a sinusoidal waveform to match the basic shape of a rectangular waveform would inherently yield the same expected plating or deplating effect--the only difference being that the current change is continuous rather than discreet.

Relevant to claims 10-11, the condition when the offset is greater than zero and wherein an absolute of the amplitude is greater than an absolute of the offset would result in a net deposition of metal on the surface, since "the cathodic-to-anodic net

charge ratio will be greater than one," or stated alternatively, the cathodic charge transfer density will be greater than the anodic charge transfer density.

Relevant to claims 12 and 33, the condition when the offset is less than zero would result in a net removal of metal on the surface, since the cathodic charge transfer density will be less than the anodic charge transfer density.

Relevant to claims 13, 32 and 34, the condition when an absolute of the amplitude is equal to an absolute of the offset is equivalent to applying a DC current--as purely cathodic when the offset is greater than zero, or purely anodic when the offset is less than zero.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Taylor et al. '384 by using sinusoidal waveform for electroplating as taught by Piersol, because it would prevent the gradual accumulation of hydrogen at the cathode surface. Furthermore, it is within the ability to one having ordinary skill in the art to modify the parameters of a sinusoidal waveform in order to achieve the same expected plating or deplating effect as compared to that from a rectangular waveform.

Claims 17, 23 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. '384 in view of Taylor et al. '528.

Taylor et al. '384 teach the method as described above in addressing claims 1-9, 14-16, 18-22, 24-30, 35-41, and 43-46. The difference between the reference to Taylor et al. '384 and the instant claims is that the reference does not explicitly teach depositing an electrically conductive seed layer by electroless plating nor having the first time interval being longer than the second time interval.

Relevant to claims 17 and 42, Taylor et al. '528 teach that "in order to prepare for the deposition of the copper layer, the surfaces to be plated, e.g., the surfaces...the interior surfaces of the vias...and the inside of the through-hole...are covered with a thin layer of a conductor by conventional procedures, e.g., by sputtering, electroless deposition, or the like" (column 9 lines 45-50).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Taylor et al. '384 by using depositing the seed layer by electroless plating as taught by Taylor et al. '528, because depositing by electroless plating is conventionally known, and because depositing the seed layer by electroless plating forms a conformal layer in order to initiate the deposition of the copper layer and to deposit the copper layer uniformly.

Relevant to claims 23, Taylor et al. '528 teach that "the cathodic pulse is relatively long and the anodic pulse is relatively short. The relatively long cathodic

pulses will deposit metal uniformly over the large features. Such pulses tend to deposit an excess of metal at the corners and peak portions of the substrate" (column 8 lines 29-40).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Taylor et al. '384 by using long cathodic pulse time and short anodic pulse time as taught by Taylor et al. '528, because it would deposit metal uniformly over the large features.

Claims 10-13 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor '144 in view of Piersol.

Taylor '144 teach the method as described above in addressing claims 1 and 19-20. The difference between the reference to Taylor '144 and the instant claims is that the reference does not explicitly teach using sinusoidal waveform.

However, using sinusoidal waveform for electroplating is well known in the art. For example, Piersol teach that by using sinusoidal waveform, "the rate of evolution of hydrogen is varied frequently and suddenly, and the gradual accumulation of hydrogen at the cathode surface is obviated. The troublesome sudden variations in plating conditions caused by such accumulations are likewise obviated" (pg. 2 lines 88-95).

Furthermore, modifying the parameters of a sinusoidal waveform to match the basic shape of a rectangular waveform would inherently yield the same expected plating or deplating effect--the only difference being that the current change is continuous rather than discreet.

Relevant to claims 10-11, the condition when the offset is greater than zero and wherein an absolute of the amplitude is greater than an absolute of the offset would result in a net deposition of metal on the surface, since "the cathodic-to-anodic net charge ratio will be greater than one" (figure 1, profiles 1-3).

Relevant to claims 12 and 33, the condition when the offset is less than zero would result in a net removal of metal on the surface (figure 1, profile 4).

Relevant to claims 13, 32 and 34, the condition when an absolute of the amplitude is equal to an absolute of the offset is equivalent to applying a DC current--as purely cathodic when the offset is greater than zero, or purely anodic when the offset is less than zero (figure 1, profile 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Taylor '144 by using sinusoidal waveform for electroplating as taught by Piersol, because it would prevent the gradual accumulation of hydrogen at the cathode surface. Furthermore, it is within the ability to

one having ordinary skill in the art to modify the parameters of a sinusoidal waveform in order to achieve the same expected plating or deplating effect as compared to that from a rectangular waveform.

Claims 16-17 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor '144 in view of Taylor et al. '528.

Taylor '144 teach the method as described above in addressing claims 1-9, 14-15, 18-30, 35-40, and 43-46.

The difference between the reference to Taylor '144 and the instant claims is that the reference does not explicitly teach depositing an electrically conductive seed layer by physical vapor deposition nor electroless plating.

Taylor et al. '528 teach that "in order to prepare for the deposition of the copper layer, the surfaces to be plated, e.g., the surfaces...the interior surfaces of the vias...and the inside of the through-hole...are covered with a thin layer of a conductor by conventional procedures, e.g., by sputtering, electroless deposition, or the like" (column 9 lines 45-50).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Taylor '144 by using depositing the seed

layer by physical vapor deposition (which is a form of sputtering) or electroless plating as taught by Taylor et al. '528, because depositing by physical vapor deposition and electroless plating is conventionally known, and because depositing the seed layer by physical vapor deposition or electroless plating forms a conformal layer in order to initiate the deposition of the copper layer and to deposit the copper layer uniformly.

Conclusion

The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure. Smith and Kovac et al. teach using sinusoidal waveform for electropolishing and electroplating.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan V. Van whose telephone number is 571-272-8521. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LVV
8/30/05

EDNA WONG
PRIMARY EXAMINER